A Technique for Interconnecting Millimeter Wave Integrated Circuits Using BCB and Bump Bonds

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***Abstract*—A low cost interconnection scheme for millimeter wave modules is presented. This technique allows the integration of hybrid components using an inexpensive micromachined silicon motherboard and benzocyclobutene (BCB) films. The excellent planarity of BCB allows vias to be formed using bumps fabricated prior to BCB application. This approach eliminates the need for laser drilling, plasma etching, and plated holes. Several representative GaAs pHEMT's were packaged using this technique. Measurements show minimal performance degradation from 1 GHz to 48 GHz.**

***Index Terms*—BCB, MCM, millimeter wave, MMIC, packaging, Si micromachining, SOP, stud bumps.**

I. Introduction

THE demand for high performance and low cost wireless communications has created the need for highly integrated systems. One integration strategy is to combine multiple integrated circuits (IC) using the system-on-a-package (SOP) approach [1]. The resulting multi-chip module (MCM) can combine multiple technologies in a very small area while improving functionality as compared to single chip or multiple package solutions.

In millimeter wave applications, packaging techniques must address unique requirements, such as very low loss and low parasitic interconnections. Commonly used wire or ribbon bonds introduce large parasitics that are difficult to control at millimeter waves. For this reason, this research has been focused on modules that do not requires wire bonds for interconnections.

Among the techniques used to create a MCM, [2] and [3] have proposed modules where monolithic microwave IC's (MMIC's) are embedded in recessed cavities, covered with laminated dielectric layers and connected with vias. These vias require expensive processing such as laser drilling, plasma etching and via plating.

In this letter, we present a low cost MCM scheme. This approach uses bumps and spun-on BCB films to eliminate the need for laser drilling and via plating. A silicon motherboard with micro-machined cavities is used as an inexpensive alternative to [3]. In order to demonstrate this scheme, several active devices were embedded in the package and characterized. Before and after measurements show little performance degradation.

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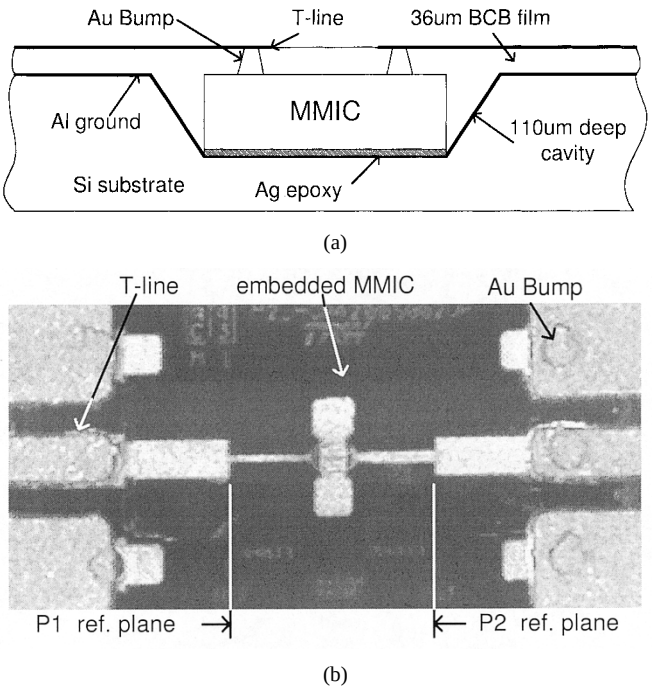


Fig. 1. (a) Cross section and (b) top view of the packaging scheme.

II. Packaging Scheme

Fig. 1(a) illustrates the cross section of the package scheme. MMIC's are precisely located by placing them in cavities etched in a low cost, low resistivity silicon substrate. The top surface of the silicon substrate is coated with a conducting film that forms a ground plane and shields the MMIC's and their interconnects from the lossy silicon below. Thus, the principle functions of the silicon are mechanical and thermal. In addition, however, the low resistivity silicon damps any parasitic modes excited between the ground plane and the base upon which the module sits. A thick multilayer BCB film is spun on top of the wafer and transmission lines are patterned on top of the BCB.

Via interconnects are formed using gold bumps. At the end of normal MMIC processing, gold bumps are formed on the contact pads much as would be done in flip chip mounting schemes. After the bumped MMIC's are mounted (bumps up) in the cavities and the BCB spun on, the bumps protrude through the BCB where they will eventually connect to the top surface transmission lines. Conducting bumps are also fabricated where necessary on the silicon surface in order to make connections between the transmission lines on top of the BCB and the ground plane on top of the silicon. Instead of batch processed plated bumps we used gold stud bumps for these prototypes.

The good planarization properties of the BCB allow it to flow around the bumps and to fill in the trenches formed between the MMIC edges and the cavity. Since the bumps are formed before the film is fabricated, no laser drilling or via plating is required. This technique reduces significantly the number of steps and cost of processing.

The MCM fabrication process is as follows.

A. Si Motherboard

The motherboard consists of a $\langle 100 \rangle$ silicon wafer supporting the MMIC cavities, the ground plane and the gold stud bump ground connections. Gold bond pads on the ground plane were necessary in this case in order to apply stud bumps for the ground vias. The following process was developed with these pads in mind.

A thin titanium layer is evaporated on the bare silicon for adhesion. Then a 0.1 μm thick gold layer is evaporated. Photoresist is applied, the contact pads are patterned and then gold plated to 3 μm thick. The evaporated layer of gold is used as a mask for silicon etching. The cavities are photo-defined, and then etched with a solution of ethylene diamine and pyrocatechol at 80 μm/hour rate. The cavities are 110 μm deep to allow space for the MMIC and silver epoxy. Then the evaporated gold is removed and stud bumps applied. Finally, aluminum is sputter deposited to a thickness of 0.5 μm over the entire surface.

B. Bump Fabrication

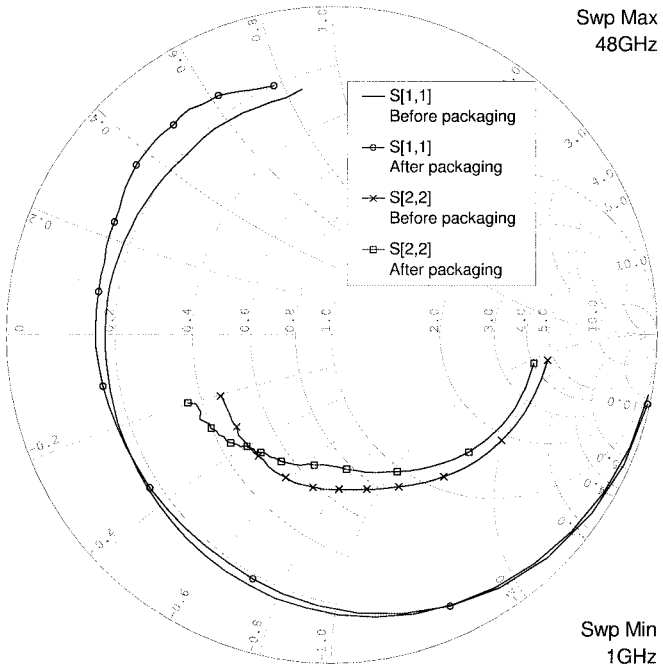
The interlayer interconnection is achieve through bumps formed before the dielectric film is applied. The bumps used for this research are stud bumps formed by ball-bonding at the contact pads and then cutting the gold wire at the desired height of 40 μm. This technique can be replaced with another more suitable for mass production such as solder bumps or gold electro-plated bumps used for flip-chip configurations. Bumps are fabricated on the MMIC as well as on the motherboard.

C. BCB Film

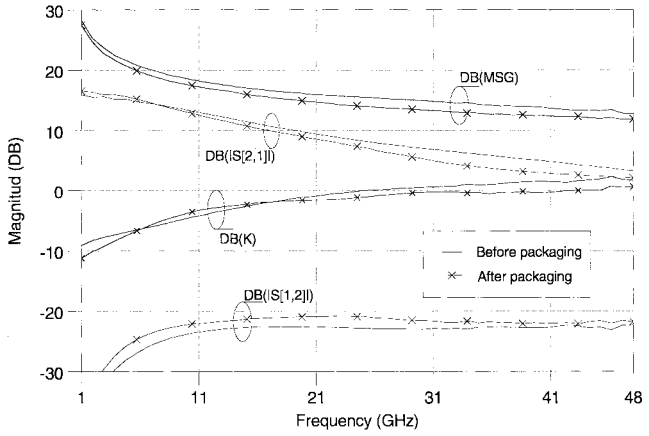
The dielectric film is formed by two 18 μm thick BCB layers (CYCLOTENE 3022–63 form Dow Chemical Co). Each layer is spun at 1500 rpm for 30 s and then cured. The cure is performed on an enclosed hot plate with flowing nitrogen to avoid oxidation of the film. The first layer is cured at 230 °C for 5 min, and the second layer at 250 °C for 60 min. With this schedule, a 98% conversion is achieved. Due to the high coefficient of thermal expansion (CTE) of BCB, special care is necessary to achieve good adhesion to the aluminum coated silicon substrate. Good aluminum-BCB adhesion is obtained using the AP3000 adhesive promoter from Dow Chemical Co.

D. Final Interconnections

Once the BCB film has been formed, a soft lapping with diamond paper removes a very small quantity of dielectric to uncover the top of the bumps. Then a short argon etching is performed and a thin sputtered copper layer deposited to enhance adhesion. Finally, gold is evaporated and then plated to achieve 3 μm thick photo-defined interconnections.



(a)



(b)

Fig. 2. Measured values of (a) S_{11} and S_{22} and (b) S_{12}, S_{21}, K–factor and MSG of an active device before and after being packeged.

III. Measurements and Analysis

The performance of MMIC's packaged using this technique may be changed by the processing described above or as a result of being embedded in BCB. In order to characterize this change several GaAs chips with single pHEMT's were packaged. One of the packaged devices is shown in Fig. 1(b) where the pHEMT is visible through the transparent BCB film. The devices were measured before and after being embedded in the package. The measurements were performed on a 8510 vector network analyzer, using 150 μm pitch microprobes.

The calibration plane was set to the end of the microprobes. The transition from the reference planes [shown in Fig. 1(b)] to the microporbes was carefully modeled and then removed from the measurement. Thus the before and after measurements shown in Fig. 2(a) are the input and output scattering parameters of the sample pHEMT referenced to the same plane.

The model of the transition consists of three parts: a section of CPW on BCB, interlayer connection (bumps) and microstrip structures on GaAs covered with BCB film. The behavior of the interlayer connection and the microstrip structures was obtained from EM simulations in the 1–50 GHz range.

Fig. 2(b) shows the stability factor (K factor), the maximum stable gain ($MSG = |S_{21}|/|S_{12}|$), $|S_{12}|$ and $|S_{21}|$ of the sample taken at the reference planes. A property of the MSG is that it will only be changed by extra feedback introduced by the packaging scheme, (principly the BCB overlayer) but will not be affected by loss in the input/output transitions. On the other hand, the K factor could be changed both by added feedback and loss in the input/output transitions. The device and measurements shown in Figs. 1(b) and 2 are from a 0.15 μm TRW GaAs pHEMT. The plots show only small change in MSG and K. Several 0.25 μm TRIQUINT GaAs pHEMT were also packaged and characterized. These devices showed similar results except for a 1 to 2 db increase in the K–factor above 40 GHz. We attribute this increase to a processing difficulty with that batch.

IV. Conclusions

This letter presents an MCM packaging scheme using micromachined silicon substrates, BCB films and preformed gold bumps. The silicon is used as a mechanical support because of its good thermal properties and because it is easily processed to enable precise die placement. BCB films are used as a dielectric due to their excellent millimeter-wave characteristics and good planarity. Preformed gold bumps were used to create via interconnections because they can be fabricated using standard batch processing techniques, but without using laser drilling or harsh plasma etching. Wire bonds are eliminated and thus interconnects are repeatable and low inductance. This is the principle contribution of this work. Using this scheme, IC's with different processing technologies (GaAs, Si, InP) can be combined with passive structures such as antennas and filters for high frequency, high performance applications

Measurements from 1 GHz to 48 GHz show that the packaging scheme introduces minimal changes in the characteristics of test pHEMT devices. These changes are likely less than or comparable to those occurring when a device is flip chip mounted with an underfill.

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